What is claimed is:

1. A memory device, comprising:

at least two cell blocks connected to a global bit line for outputting data in response to an instruction;

at least one global bit line connection unit for selectively connecting the global bit line to each cell block under control of a control block, one global bit line connection unit being allocated between the two cell blocks; and

said control block for controlling output of data stored in each cell block to the global bit line and restoration of the outputted data of the global bit line to the original cell block or another cell block which is determined by depending upon whether data in response to a next instruction is outputted from the original cell block or another cell block.

2. The memory device as recited in claim 1, wherein each cell block includes:

a first cell array including a plurality of unit cells and outputting data;

a first bit line sense amplifier block for amplifying data outputted from the first cell array and outputting the amplified data to the global bit line; and

a first bit line sense amplifier connection unit for connecting the first cell array to the first bit line sense amplifier block and disconnecting the first cell array to the

first bit line sense amplifier block as soon as the data are sensed in the first bit line sense amplifier block.

3. The memory device as recited in claim 2, wherein each cell block includes:

a second bit line sense amplifier block for amplifying data inputted from the global bit line; and

a second bit line sense amplifier connection unit for connecting or disconnecting the first cell array to the second bit line sense amplifier block.

4. The memory device as recited in claim 3, further comprising a latch means for transiently latching the data supplied to the global bit line in response to the instruction.

5. The memory device as recited in claim 4, wherein the control block controls to restore the data latched by the latch means in the first cell block and to read another data stored in the first cell block or another cell block in response to the next instruction at a substantially simultaneous timing period.

6. The memory device as recited in claim 5, wherein the control block controls to output the data latched by the latch means in response to the active instruction.

7. A memory device, comprising:

a plurality of unit cell blocks, each having a plurality of unit cells, a first local bit line sense amplifier block for sensing and amplifying data from a unit cell, and a second local bit line sense amplifier block for sensing and amplifying data from another cell unit;

a first global bit line sense amplifier block for latching data sensed and amplified from the first local bit line sense amplifier block;

a second global bit line sense amplifier block for latching data sensed and amplified from the second local bit line sense amplifier block;

a first global bit line connection unit, in response to a first control signal, for selectively connecting either the second local bit line sense amplifier block of a first unit cell block to the second global bit line sense amplifier block or the first local bit line sense amplifier block of a second unit cell block to the first global bit line sense amplifier block;

a second global bit line connection unit, in response to a second control signal, for selectively connecting either the second local bit line sense amplifier block of a third unit cell block to the second global bit line sense amplifier block or the first local bit line sense amplifier block of a forth unit cell block to the first global bit line sense amplifier block; and

a control means for generating the control signals to

thereby control a storing operation of the data latched in the first and the second global bit line sense amplifier block.

8. The memory device as recited in claim 7, wherein the control means controls to restore a first data not in the first unit cell but in the other unit cell block and access a second data in the first unit cell block when the first and the second data are accessed in the first unit cell block.

9. The memory device as recited in claim 8, wherein the control means controls to restore a first data in the first unit cell block and access a second data in the second unit cell block at substantially simultaneous timing period, when the first and the second data are accessed by turns in the first and the second unit cell blocks.

10. The memory device as recited in claim 9, wherein the control means controls to output the data selected in data latched in the first and the second global bit line sense amplifier blocks in response to an active read instruction.

11. The memory device as recited in claim 8, further comprising a third global bit line connection unit, in response to a third control signal, for selectively connecting the second local bit line sense amplifier block of a fifth unit cell block to the second global bit line sense amplifier block.

12. The memory device as recited in claim 11 further comprising a global bit line for either delivering data sensed and amplified by the first local bit line sense amplifier block to the first global bit line sense amplifier block or directly delivering data sensed and amplified by the second local bit line sense amplifier block to the second global bit line sense amplifier block.

13. The memory device as recited in claim 12, wherein the first and the second local bit line sense amplifier blocks have individually a switching means for connecting to either one of the first to the third global bit line connection units or the global bit line.

14. A memory device, comprising:

a plurality of first unit cell blocks, each having a plurality of unit cells, a first local bit line sense amplifier block for sensing and amplifying data from a unit, and a second local bit line sense amplifier block for sensing and amplifying data from another unit cell;

a first global bit line sense amplifier block for latching data sensed and amplified by the first local bit line sense amplifier block;

a second global bit line sense amplifier block for latching data sensed and amplified by the second local bit line sense amplifier block; and

a control means for controlling a restoration execution

of data latched in the first and the second global bit lines.

15. The memory device as recited in claim 14, wherein the control means controls an operation that not a first data is restored in a first unit cell block but a second data is accessed in the first unit cell block and the first data is restored in the other unit cell block except the first unit cell block, when the first and the second data are continuously accessed in the first unit cell block.

16. The memory device as recited in claim 15, wherein the control means controls operation that a first data is restored in the first unit cell block and a second data is accessed in the second unit cell block at a substantially simultaneous timing period, when the first and the second data are accessed by turns in the first and the second unit cell blocks.

17. The memory device as recited in claim 16, wherein the control means controls to output data selected between the data latched in the first and the second global bit lines in response to an active read instruction.

18. The memory device as recited in claim 17, further comprising:

a first global bit line for delivering the data sensed and amplified by the first local bit line sense amplifier block to the first global bit line sense amplifier block; and

a second global bit line for connecting the second local bit line sense amplifier to the second global bit line sense amplifier.

19. The memory device as recited in claim 18, wherein the first local bit line sense amplifier block has a first switching means for selectively connecting the first local bit line sense amplifier block to the first global bit line, and the second local bit line sense amplifier block has a second switching means for selectively connecting the second local bit line sense amplifier block to the second global bit line.

20. A memory device, comprising:

a plurality of unit cell blocks, each including a local bit line sense amplifier block for sensing and amplifying data stored in a plurality of unit cells and having the plurality of the unit cells;

a global bit line sense amplifier block for latching data sensed and amplified by the plurality of the local bit line sense amplifier block; and

a control means for controlling the use of the latched data in a restoration execution.

21. The memory device as recited in claim 20, wherein each of the local bit line sense amplifier blocks includes a switching means for selectively connecting each of the local bit line sense amplifier blocks to the global bit line sense

amplifier block.

22. The memory device as recited in claim 21, wherein the control means controls to access a second data in a first unit cell block and to restore a first data not in the first unit cell block but in the other unit cell block, when the first and the second data are continuously accessed in the first unit cell block selected in the plurality of the unit cell blocks.

23. The memory device as recited in claim 22, wherein the control means controls to restore a first data in the first unit cell block and to access a second data in the second unit cell block at a substantially simultaneous timing period, when the first and the second data are accessed by turns in the first and the second unit cell blocks.

24. The memory device as recited in claim 23, wherein the control means controls to output data latched in the global bit line sense amplifier block in response to an active read instruction.

25. The memory device as recited in claim 20, wherein the global bit line sense amplifier block includes:

a first global bit line sense amplifier block for latching data sensed and amplified by the local bit line sense amplifier block; and

a second global bit lin sense amplifier block for latching the other data sensed and amplified by the local bit line sense amplifier block.

26. The memory device as recited in claim 25, wherein the control means control to access a second data in the first unit cell block and to restore a first data not in the first unit cell block but in the other unit cell block, when the first and the second data is continuously accessed in the first unit cell block selected out of the plurality of the unit cell blocks.

27. The memory device as recited in claim 26, wherein the control means controls to restore a first data in the first unit cell block and to access a second data in the second unit cell block at a substantially simultaneous timing period, when the first and the second data are accessed by turns in the first and the second unit cell blocks.

28. The memory device as recited in claim 27, wherein the control means controls to output the data latched in the first and the second global bit line sense amplifier blocks in response to the active read instruction.

29. The memory device as recited in claim 27, further comprising a global bit line for connecting the plurality of the local bit line sense amplifier blocks to the first and

second global bit line sense amplifier blocks.

30. A memory device, comprising:

a cell area including N+1 number of unit cell blocks, each having M number of word lines for responding to inputted row address; and

a control means for controlling the cell area to thereby restoring data accessed in a first unit cell block selected out of the N+1 number of the unit cell blocks either in the first unit cell block or in a second unit cell block.

31. The memory device as recited in claim 30, wherein the control means control to activate each word line of two unit cell blocks in response to the inputted row address.

32. The memory device as recited in claim 31, wherein each address for selecting each word line activated in the two unit cell blocks is the same address.

33. The memory device as recited in claim 32, wherein the control means controls to access a second data in the first unit cell block and to restore a first data not in the first unit cell block but in the second unit cell block, when the first and second data are continuously accessed in the first unit cell block.

34. The memory device as recited in claim 33, wherein the

control means controls to restore a first data in the first unit cell block and to access a second data in the second unit cell block at substantially simultaneous timing period, when the first and the second data are accessed by turns in the first and the second unit cell block.

35. The memory device as recited in claim 34, wherein the cell area further includes a global bit line sense amplifier block for latching the data sensed and amplified by the local bit line sense amplifier block individually located in the N+1 number of the unit cell blocks.

36. The memory device as recited in claim 35, wherein the cell area further includes a global bit line connection unit for selectively connecting the local bit line sense amplifier block to the global bit line sense amplifier block.

37. The memory device as recited in claim 34, wherein the cell area further includes a global bit line for connecting the local bit line sense amplifier block to the global bit line sense amplifier block.

38. The memory device as recited in claim 36, wherein the control means control to allow data latched in the global bit line sense amplifier output data in response to active read instruction.

39. A memory device, comprising:

a cell area having N+1 number of unit cell blocks, each including M number of word lines for responding to an inputted row address;

a predetermined cell block table for storing information wherein at least more than one word line among the (N+1)×M number of the word lines is assigned as a predetermined restorable word line by using the information;

a tag block for sensing an input logical cell block address for designating a unit cell block to be accessed to converting the input logical cell block address into a physical cell block address for designating a unit cell block to be restored; and

a control means for controlling the tag block and the predetermined cell block table for activating one word line of the unit cell block selected by the physical cell block address.

40. The memory device as recited in claim 39, wherein the control means controls an operation that a first data is restored by the selected predetermined word line when the first and a second data are continuously accessed in one unit cell block selected in the N+1 number of the unit cell blocks.

41. The memory device as recited in claim 40, wherein a number of the predetermined word lines are M.

42. The memory device as recited in claim 41, wherein the tag block including:

an N+1 number of unit tag tables, each storing information that M number of word lines included in each of N+1 number of unit cell blocks correspond to the logical cell block;

a N+1 number of comparators for comparing information-N+1 of data information about which the logical unit cell block corresponds to the word line selected by the local row address outputted from the N+1 number of the unit tag tables in response to a local address for selecting one word line of the unit cell block with the logical cell block address sensed by the row address;

a encoder for outputting the physical cell block address by encoding information compared by the N+1 number of comparators; and

a tag control block for controlling the N+1 number of the unit tag tables, the N+1 number of the comparators, and the encoder.

43. The memory device as recited in claim 42, wherein the tag block further includes a cell block address decoder for outputting to one unit tag table selected in the N+1 number of the unit tag tables by decoding information wherein unit cell block of the N+1 number of the unit cell blocks has the predetermined word line corresponding to the word line sel cted by the local address outputted from the predetermined

cell block table.

44. The memory device as recited in claim 43, wherein the predetermined cell block table has M number of registers for storing information what unit cell block out of the N+1 number of the physical unit cell blocks has the M number of the predetermined word line.

45. The memory device as recited in claim 44, wherein the control means controls an operation that a second data is accessed and a first data is restored not in a first unit cell block but in a second unit cell block being different from the first unit cell block when the first and the second data are continuously accessed in the first unit cell block selected in the N+1 number of the unit cell blocks.

46. The memory device as recited in claim 45, wherein the control means controls an operation that a second data is accessed in a second unit cell block at a substantially simultaneous timing period in which a first data is restored in a first unit cell block when the first and the second data are accessed in the first and the second unit cell blocks by turns.

47. The memory device as recited in claim 46, wherein the cell area includes a data latch block for latching the data sensed and amplified by the local bit line sense amplifier

block included in each of the N+1 number of the unit cell blocks.

48. The memory device as recited in claim 47, wherein the control means controls an operation that the data latched in the data latch block is outputted in response to an active read instruction.

49. The memory device as recited in claim 47, wherein the cell area includes a global bit line connection unit for selectively connecting the data latch block to the local bit line sense amplifier block included in each of the N+1 number of the unit cell blocks.

50. A memory device, comprising:

a cell area including N+1 number of unit cell blocks adding N number of the unit cell blocks individually having M number of word lines for responding to an inputted row address and an additional unit cell block having M number of the word lines;

a data access control means for controlling operation that data accessed in a first unit cell block selected in the N+1 number of the unit cell blocks are restored either in the first unit cell block or in a second unit cell block; and

an instruction control means for controlling an operation that a cell block address in response to a second instruction being at an active next timing period is converse and a bit

line in response to a first instruction is precharged during accessing data in response to the first present active instruction.

51. The memory device as recited in claim 50, wherein the data access control means controls an operation that not a first data is restored in a first unit cell block but a second data is accessed in the first unit cell block and the first data is restored in the firs unit cell block, when the first and the second data is continuously accessed in the first unit cell block.

52. The memory device as recited in claim 51, wherein the data access control means controls an operation that a second data is accessed in the second unit cell block at a timing period when a first data is restored in the first unit cell block when the first and second data are alternatively accessed in the first and the second unit cell blocks.

53. The memory device as recited in claim 52, wherein the control means including:

a cell block address convert means for sensing a logical cell block address from an inputted low address in response to a first instruction and thereof converting it to a physical cell block address for selecting one out of the N+1 number of the unit cell blocks;

a precharge control block for precharging data sensed and

amplified by the first instruction; and

an instruction timing control block for controlling the precharge control block for operating the forced precharge execution in response to the first instruction after latching the data sensed and amplified by the first instruction.

54. The memory device as recited in claim 53, wherein the instruction timing control block includes a delay block for delaying a second instruction during a time of converting the cell block address in response to the second instruction and the forced precharge execution in response to the first instruction and thereof outputting, and controls the data access control means for operating the sensing and amplifying execution of data in response to the second instruction by the second instruction delayed by the delay block.

55. The memory device as recited in claim 54, wherein the cell area includes a data latch block for latching the data sensed and amplified in a local bit line sense amplifier block included in each of the N+1 number of the unit cell blocks.

56. The memory device as recited in claim 55, wherein the control means controls to allow the data latched in the data latch block output data in response to an active read instruction.

57. Th memory device as recited in claim 56, wherein the

cell area includes a global bit line connection unit for selectively connecting the data latch block to the local bit line sense amplifier block included in each of the N+1 number of the unit cell blocks.

58. The memory device as recited in claim 57, wherein the cell area includes a global bit line for connecting the data latch block to the local bit line sense amplifier block included in each of the N+1 number of the unit cell blocks.

59. A method for operating a memory device having first and second cell blocks, each having a number of cell units, comprising the steps of:

(A) sensing and amplifying a first data in the first cell block;

(B) restoring the first data in the second cell block; and

(C) sensing and amplifying a second data in the first unit block,

wherein both the step (B) and the step (C) are performed at a substantially simultaneous timing period.

60. The method for operating the memory device as recited in claim 59, wherein the step (B) includes the steps of:

(L) moving the first data and latching thereof; and

(M) moving the latched first data to the second cell

block and restoring thereof.

61. The method for operating the memory device as recited in claim 60, further comprising the step of (N) outputting the first data latched by the step (L) in response to an inputted read instruction.

62. A method for operating a memory device having an N+1 number of unit cell blocks adding an N number of unit cell blocks and an additional unit cell block individually both corresponding to an inputted row address and having an M number of word lines, N and M being positive integers, comprising steps of:

(A) sensing and amplifying a first data in a first unit cell block selected out of the N+1 number of the unit cell blocks;

(B) restoring the first data in a second unit cell block selected out of the N+1 number of the unit cell blocks; and

(C) sensing and amplifying a second data in the first unit cell block,

wherein both the step (B) and the step (C) are performed at a substantially simultaneous timing period.

63. The method for operating the memory device as recited in claim 62, wherein the step (B) includes the steps of:

(K) moving the first data and latching thereof; and

(L) moving the latched first data to the second unit cell block and restoring thereof.

64. The method for operating the memory device as recited in claim 63, further comprising the step of (M) outputting the first data latched by the step K in response to an inputted read instruction.

65. The method for operating the memory device as recited in claim 64, further comprising the step of (N) precharging the first sensed and amplified data and deleting thereof, after the first data is latched.

66. A method for operating a memory device including an N+1 number of unit cell blocks, adding a N number of unit cell blocks and an additional unit cell block, both corresponding to an inputted row address and having a M number of word lines, N and M being positive integers, comprising the steps of:

(A) activating a first word line of a first unit cell block selected out of the N+1 number of the unit cell blocks;

(B) sensing and amplifying a K number of data in response to the first word line;

(C) moving the K number of the sensed and amplified data in response to the first word line to the other unit cell block having a predetermined word line in response to the first word line and restoring thereof;

(D) activating a second word line of the first unit cell

block;

(E) sensing and amplifying a K number of data in response to the second word line,

wherein the steps (C) and (E) are performed at substantially simultaneous timing period.

67. The method for operating the memory device as recited in claim 66, wherein the step (C) includes the steps of:

(H) moving a K number of the data in response to the first word line and latching thereof;

(I) activating a predetermined word line in response to the first word line; and

(J) restoring the K number of the latched data in a K number of the unit cells in response to the predetermined word line.

68. The method for operating the memory device as recited in claim 67, wherein the step (H) includes the step of (k) outputting one selected out of the K number of latched data in response to an inputted read instruction.

69. The method for operating the memory device as recited in claim 68, further comprising the step of (L) precharging data supplied to a bit line in response to the first word line and deleting thereof, after the data is sensed and amplified.

70. A m thod for operating a memory device having a cell

ar a containing an N+1 number of unit cell blocks, adding an N number of unit cell blocks and an additional unit cell block, both corresponding to an inputted row address and having an M number of word lines, N and M being positive integers, comprising the steps of:

(A) sensing data by both a logical cell block address for selecting a N number of logical unit cell blocks by receiving the row address and a local address for selecting one out of the M number of word lines included in the selected unit cell block;

(B) converting the logical cell block address to a physical cell block address for selecting one out of a N+1 number of the physical cell block addresses;

(C) activating a first word line in response to the local address in a first unit cell block selected in response to the converted physical cell block address;

(D) sensing and amplifying the data in response to the first word line;

(E) moving the first data to a second unit cell block of which a predetermined word line is assigned in response to the first word line;

(F) activating a second word line of the first unit cell block in response to the local address inputted for a next instruction; and

(G) sensing and amplifying a second data in response to the second word line,

wherein the steps E and G are occurred at a substantially

simultaneous timing period.

71. The method for operating the memory device as recited in claim 70, wherein the step (E) includes the steps of:

(O) moving the first data to the first word line and latching thereof;

(P) activating the predetermined word line in response to the first word line; and

(Q) of restoring the first latched data in the cell unit in response to the predetermined word line.

72. The method for operating the memory device as recited in claim 71, further comprising the step of (H) outputting the first data latched in the step O in response to an inputted read instruction.

73. The method for operating the memory device as recited in claim 72, further comprising the step of (I) precharging the first data supplied to the bit line by being sensed and amplified in response to the first word line.

74. The method for operating the memory device as recited in claim 73, wherein the first word line and the predetermined word line are selected by the same row address.

75. A method for operating a memory device including a cell area having an N+1 number of unit cell blocks, adding an

N number of unit cell blocks and an additional unit cell block, individually both corresponding to an inputted logical cell block address and having an M number of word lines, N and M being positive integers, comprising the steps of:

(A) receiving a first logical cell block address in response to a first instruction and thereof converting to a first physical cell block address for selecting one out of a N+1 number of the physical cell block addresses;

(B) sensing and amplifying a first data in a first unit cell block in response to the first physical cell block address;

(C) moving the first data and latching thereof;

(D) precharging the first data sensed and amplified in the first unit cell block;

(E) converting to a second physical cell block address after receiving a second logical cell block address in response to a second instruction;

(F) moving the first latched data to the second unit cell block selected out of the N+1 number of the unit cell blocks and restoring thereof; and

(G) of sensing and amplifying the second data in the second unit cell block in response to the second physical cell block address,

wherein the steps F and G are occurred at a substantially simultaneous timing period.

76. The method for operating the memory device as recited

in claim 75, further comprising the step of (H) delaying th second instruction for a time of operating the steps D and E and receiving thereof, and also includes the step G is occurred using the second instruction delayed by the step H.

77. The method for operating the memory device as recited in claim 75, further comprising the step of (I) outputting the first data latched in the step C in response to an inputted read instruction.